of 0.4 μm as field oxide film **12** to protect the surface of a peripheral voltage-withstanding structure that surrounds the active portion. As shown in FIG. **1**J, that portion of the HTO film which corresponds to the active portion where a main current of the device is to flow is removed by photolithography and etching. Then, a 1,000-Å-thick gate oxide film **13** is grown at 900° C. and 0.5 μm-thick polysilicon to become gate electrodes **14** is deposited thereon. As shown in FIG. **1**K, windows are formed through the polysilicon layer by patterning and RIE. Then, as shown in FIG. **1**L, a 1.1-μm-thick BPSG (boro-phospho silicate glass) is grown as an interlayer insulating film **15** and contact holes **16** are formed by patterning and etching. Then, a 5-μm-thick Al—Si layer is grown as source electrode **17**. After the Al—Si layer is patterned, a polyimide protective film **18** is formed as shown in FIG. **1**M. After the back surface of the silicon substrate is ground, a back drain electrode (lamination film) is formed by evaporating Ti, Ni, and Au, for example. The wafer process is thus completed.

[**0040**] In the first embodiment, the MOS gate structures including p-type base regions **6** and the n-type source regions **7** are formed before formation of the SJ column structure. Therefore, the SJ column structure is subjected to a smaller number of thermal history events and hence the mutual impurity diffusion between p-type regions (columns) **3** and n-type regions **2** (columns) is suppressed. The breakdown-voltage-related yield can thus be increased.

Embodiment 2

[**0041**] FIG. **3** is a sectional view of an important part of a trench gate SJ-MOSFET according to the second embodiment of the invention. As shown in FIG. **3**, this SJ-MOSFET is manufactured in the following manner. A 50-μm-thick n-type silicon epitaxial layer **22** is grown on a low-resistivity n^+ silicon substrate **21**. Boron ions are implanted into a surface active region (where a main current of the device is to flow) of epitaxial layer **22** and diffused at 1,150° C. for 3 hours in an oxidizing atmosphere, whereby p-type base region **23** of 2 μm in depth is formed. A mask oxide film (not shown) is formed by patterning, by photolithography, a thermal oxide film that was formed on the surface when p-type base region **23** was formed. Anisotropic etching is performed on the non-masked opening portions from the front side by reactive ion etching (RIE), whereby trenches **24** of 1.5 μm in width and 2.5 μm in depth are formed at intervals of 12 μm so as to penetrate through p-type base region **23** and reach n-type epitaxial layer **22**. After the sacrificial oxide film and the mask oxide film are removed, gate oxide films **25** are formed on the surfaces of the trenches. Then, gate electrodes **26** are formed by burying deposited polysilicon layers in the respective trenches. After patterning is performed, n^+ source regions **27** are formed in substrate surface regions adjacent to the openings of trenches **24** by ion-implanting and diffusing an n-type dopant.

[**0042**] After a CVD oxide film is deposited and an oxide film mask pattern is formed, trenches of 6 μm in width and 50 μm in depth are formed through p-type base regions **23** between trenches **24** by performing anisotropic RIE from the front side. Then, as in the first embodiment, p-type epitaxial silicon **28** is buried in the respective trenches **24** while trichlorosilane, hydrogen, diborane, and hydrogen chloride are supplied simultaneously. The front surface is planarized by chemical mechanical polishing (CMP) which is stopped when the mask oxide film is exposed. Surface-exposed silicon is etched away, whereby the steps of the silicon surface are reduced in height and the silicon surface is thereby made approximately flat. SJ columns **22** and **28** are thus formed. Then, boron ions are implanted at 3×10^{15} cm^{-2} after a resist is applied and patterned. After the resist is removed, annealing is performed at 1,100° C. for 1 hour, whereby high-impurity-concentration second p^+ regions **29** are formed. Then, as in the first embodiment, interlayer insulating film **30**, source metal electrode **31** (formed on interlayer insulating film **30**), a back drain electrode (not shown), etc. are formed. The wafer process is thus completed.

[**0043**] In the second embodiment, as in the case of the first embodiment, the MOS gate structures including p-type base regions **6**, n-type source regions **7**, channels (not shown), and gate oxide films **25** are formed before formation of the SJ column structure. Therefore, the SJ column structure is subjected to a smaller number of thermal history events and hence the mutual impurity diffusion between p-type regions **28** (columns) and n-type regions **22** (columns) is suppressed. The breakdown-voltage-related yield can thus be increased.

[**0044**] Thus, a manufacturing method of a super-junction semiconductor device has been described according to the present invention. Many modifications and variations may be made to the techniques and structures described and illustrated herein without departing from the spirit and scope of the invention. Accordingly, it should be understood that the methods described herein are illustrative only and are not limiting upon the scope of the invention.

What is claimed is:

1. A method of manufacturing a super-junction semiconductor device comprising, in order:

(a) depositing, on a low-resistivity semiconductor substrate of a first conductivity type, at least an epitaxial layer of the first conductivity type which is to become a drift layer;

(b) forming at least one base region of a second conductivity type and source region of the first conductivity type to be used for formation of MOS gate structures in an active portion where a main current is to flow;

(c) forming, by anisotropic etching using an insulating film mask, trenches that penetrate through the at least one base region and reach the low-resistivity semiconductor substrate or its vicinity; and

(d) burying epitaxial layers of the second conductivity type in the respective trenches.

2. The method according to claim 1, wherein (b) comprises forming a base region of the second conductivity type and then forming trench MOS gate structures including source regions of the first conductivity type, and (c) comprises forming trenches between the trench MOS gate structures from the surface of the base region by performing anisotropic etching using an insulating film mask, wherein the trenches are deeper than the base region and penetrate through the base region and reach the low-resistivity semiconductor substrate or its vicinity, and wherein gate oxide films cover side walls of the trenches, and gate electrodes are buried in the trenches.